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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/842,332	04/24/2001	Wai Fong	5181-76300	7536

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EXAMINER
HA, DAC V

ART UNIT	PAPER NUMBER
2634	4

DATE MAILED: 07/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/842,332	FONG ET AL.	
	Examiner	Art Unit	
	Dac V. Ha	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2,3*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 1-17 are objected to because of the following informalities:

Claim 1, line 9, the recitation "clock buffer" should be changed to "clock signal buffer" to be consistent.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 18-34 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 18 recites "said receiving" on line 6, it is not clear what receiving step it refers to since there are two receiving steps (i.e., "receiving the first clock signal" and "receiving a clock detect signal").

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 1-34** are rejected under 35 U.S.C. 103(a) as being unpatentable over Knoll et al. (US 6,233,200) (hereinafter Knoll) in view of Yamazaki et al. (US 6,198,689) (hereinafter Yamazaki).

Regarding claim 1, Knoll discloses the claimed subject matter

"a clock receiver comprising a clock signal buffer and a clock detector, wherein the clock signal buffer is configured to receive a first clock signal and drive a second clock signal responsive to receiving the first clock signal, and wherein the clock detector is configured to assert a clock detect signal responsive to receiving the first clock signal;

a" "locked loop" "circuit configured to receive the second clock signal from the clock buffer, wherein the DLL circuit is configured to drive the second clock signal to the data buffer; a clock verification circuit, wherein the clock verification circuit is configured to receive the clock detect signal from the clock detector" including receiving "a first clock signal" (Figure 5, element 502; Col. 3, lines 22-23); and generating "a second clock" using a PLL (Figure 3, element 206; Figure 5, element 502;) and "a clock verification circuit" (Figure 3, element 308) for controlling the distribution of clocks based on lock detection (Col. 2, lines 54-64). In Knoll, the determination of a lock condition also determines detection of the first clock.

Knoll differs from the claimed invention in that it doesn't teach the claimed subject matter "a data buffer configured to receive data through one or more signal lines", "a DLL" and "wherein the clock verification circuit is configured to reset the source synchronous receiver responsive to a failure to receive clock detect signal". Knoll discloses driving a load using the distributed clock. Yamazaki discloses

controlling data transfer via a "data buffer" using a "DLL" (Figure 2, elements 2, 3). Therefore, the use of "DLL" and "data buffer" would have been realized by one skilled in the art as obvious since using DLL is more reliable and data buffer provides more control capability to the data flow. Further, Knoll discloses a concept of taking an appropriate action (i.e., disabling the distributing of clock in one embodiment) based upon a "verification" process. The appropriate action also includes, but not limit to, turning off certain component in the distribution network (Col. 2, line 43-52). Therefore, the claimed subject matter "wherein the clock verification circuit is configured to reset the source synchronous receiver responsive to a failure to receive clock detect signal" would have been obvious to one skilled in the art based on the above discussion for, at least, saving power consumption.

Regarding claim 18, see claim 1 above.

Regarding claims 2-7, 19-34, all these claimed subject matter would have been realized by one skilled in the art as design specific based on Knoll and Yamazaki.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Baltar (US 6,209,069) discloses Method And Apparatus Using Volatile Lock Architechture For Individual Block Locking On Flash Memory.

Mozdzen et al. (US 5,774,001) dsiclose Method For Eleiminating Multiple Output Switching Timing Skews In A Source Synchronous Design.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dac V. Ha whose telephone number is 703-306-5536. The examiner can normally be reached on 5/4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 703-305-4714. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dac V. Ha
Examiner
Art Unit 2634